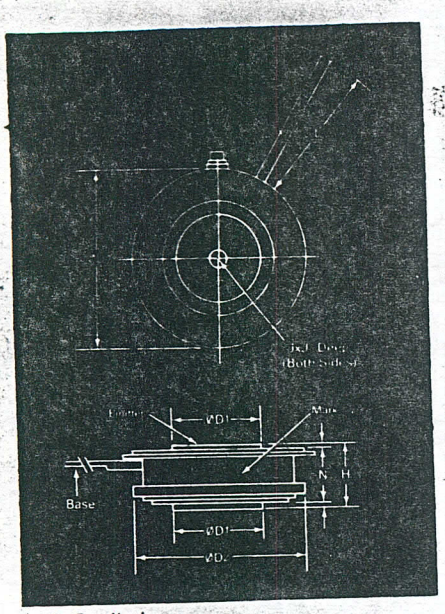
NPN Power Switching TRANSISTORS D62T

200 Amperes 400--500 Volts

September 1979

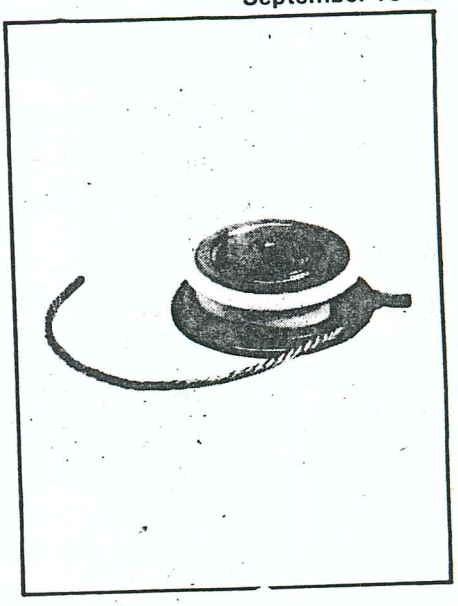


D62 Outline

Symbol	Inches		Millimeters	
	Min.	Max.	Min.	Max.
ϕD	1.610	1.650	40.89	41.91
ϕD_1	.745	.755	18.92	19.18
ϕD_2	1.420	1.460	36.07	37.08
H	.500	.560	12.70	14.22
ϕJ	.135	.145	3.43	3.68
J_1	.072	.082	1.83	2.08
L	4.000		101.6	
N	.030		.76	

Creep Distance—.34 in. min. (8.64mm)
Strike Distance—.52 in. min. (13.21mm)
(In accordance with NEMA standards.)
Finish—Nickel Plate.
Approx. Weight—2.1 oz. (60 g).
1. Dimension "H" is a clamped dimension.

2. "Base Lead is No. 14 uninsulated flexible stranded wire.



Maximum Ratings
Collector Current (peak): 200 Amperes
Collector Current (continuous): 200 Amperes
Base Current (continuous): 20 Amperes
Power Dissipation: 1100 Watts at T_C = 75°C
Operating and Storage Temperature: -65°C to 200°C

Applications
- High Frequency Inverters
- Motor Controls
- Switching Regulators
- VLF Transmitters
- Induction Heating Power Supplies

Features
- Triple Diffused Design
- CBE Construction
- Double Sided Cooling
- Fast Switching

Ordering Information

Type	$V_{CEO(SUS)}$ (Volts)	Current Rating – Amperes			Gain
		40	50	60	
D62T	400	4040	4050	4060	10
	450	4540	4550		10
	500	5040			10

Example: Select the complete ten digit device part number you desire from the shaded area in the table above – i.e. a D62T454010 Describes a Disc Package Transistor rated at 450 Volts, 40 Amperes, and a gain of 10 at rated current (40 Amperes).

New Information 9/79

200 Amperes
400 - 500 Volts

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Electrical and Mechanical Characteristics (TCASE = 25°C unless otherwise specified)

Symbol	Characteristic		Test Conditions	Min.	Typ.	Max.	Units
$V_{CEO(SUS)}$	Collector-Emitter Sustaining Voltage		I_C = 200mA I_B = 0 Note 1		See Ordering Information on Previous Page		Volts
I_{CEV}	Collector Cutoff Current (Base Emitter Reverse Biased)		At Rated $V_{CEO(SUS)}$ + 50V $V_{BE(OFF)}$ = 1.5V,		0.1	1	mA
I_{CEV}	Collector Cutoff Current (Base Emitter Reverse Biased)		At Rated $V_{CEO(SUS)}$ + 50V $V_{BE(OFF)}$ = 1.5V, T_C = 150°C		0.8	3	mA
I_{EBO}	Emitter Cutoff Current		V_{EB} = 7V		2	30	mA
h_{FE}	DC Current Gain		I_C = Gain Rated, V_{CE} = 2.5V	10	15		
h_{FE}	DC Current Gain D62TXX40		I_C = 80A, V_{CE} = 2.5V		5		
h_{FE}	DC Current Gain D62T—50		I_C = 100A, V_{CE} = 2.5V		5		
h_{FE}	DC Current Gain D62T—60		I_C = 120A, V_{CE} = 2.5V		5		
$V_{CE(SAT)}$	Collector-Emitter Saturation Voltage		I_C = Gain Rated, I_C/I_B = 8.33		75	1.25	Volts
$V_{BE(SAT)}$	Base-Emitter Saturation Voltage		I_C/I_B = 8.33 D62T_40 D62T_50 D62T_60		1.0 1.15 1.30	1.40 1.50 1.60	Volts
t_d	Turn-On Delay	Resistive Load Switch Times	V_{CC} = 250V, I_C = 40A I_{B1} = I_{B2} = 6A t_p = 50 us Duty Cycle < 2% D62T—40			110	ns
t_r	Rise Time				0.7	1.0	µs
t_s	Storage Time				1.7	3.0	µs
t_f	Fall Time				0.3	0.5	µs
t_d	Turn-On Delay	Resistive Load Switch Times	V_{CC} = 250V, I_C = 50A I_{B1} = I_{B2} = 7.5A t_p = 50 us Duty Cycle < 2% D62T—50			120	ns
t_r	Rise Time				0.8	1.10	µs
t_s	Storage Time				1.75	3.0	µs
t_f	Fall Time				0.32	0.5	µs
t_d	Turn-On Delay	Resistive Load Switch Times	V_{CC} = 250V, I_C = 60A I_{B1} = I_{B2} = 9A t_p = 50 us Duty Cycle < 2% D62T—60			150	ns
t_r	Rise Time				0.85	1.20	µs
t_s	Storage Time				2.0	3.0	µs
t_f	Fall Time				0.35	0.5	µs
C_{OB}	Output Capacitance		f_{TEST} = 1 MHz, V_{CB} = 10V		2500		µµf
f_T	Gain-Bandwidth Product		f_{TEST} = 1 MHz, I_C = 5A, V_{CE} = 10V	7	10		MHz
$R\theta JC$	Thermal Resistance Junction to Case Double Sided Cooling		V_{CE} = 20V			0.09	°C/W
$R\theta CS$	Thermal Resistance Case to Sink Double Sided Cooling		V_{CE} = 20V, Lubricated			0.05	°C/W
	Mounting Force			900		1100	lb.
				4.05		4.95	KN

1. $V_{CEO(SUS)}$ must not be measured on a curve tracer.

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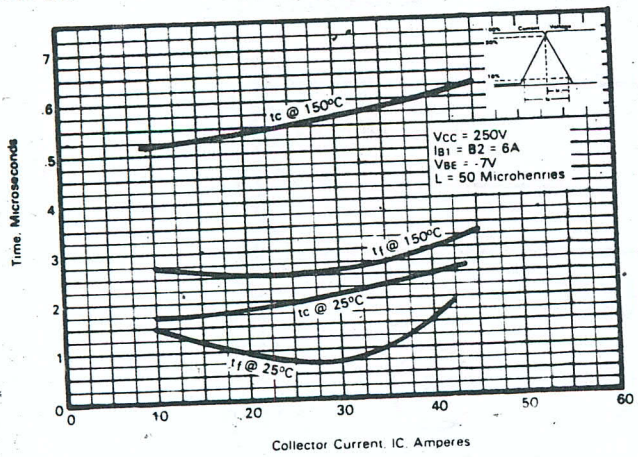
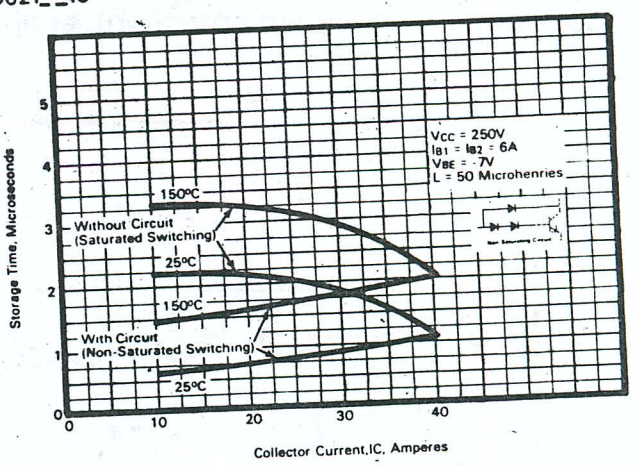
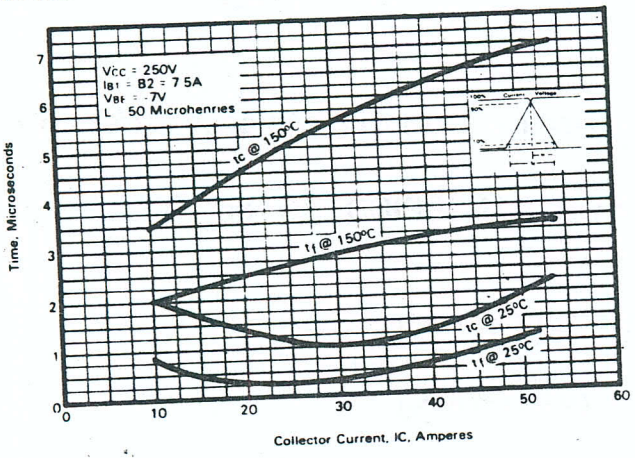
D62T_ _40 Typical Turn—Off Time For Clamped Inductive Switching



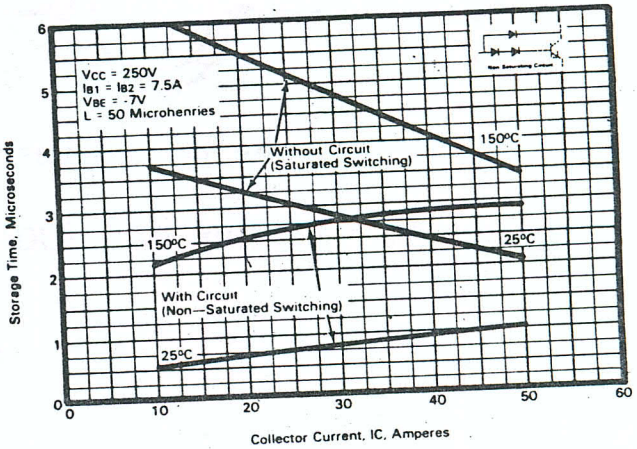
D62T_ _40 Typical Storage Time For Clamped Inductive Switching



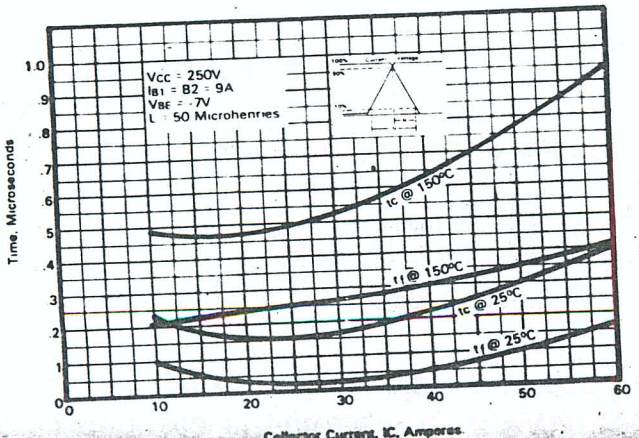
D62T_ _50 Typical Turn—Off Time For Clamped Inductive Switching



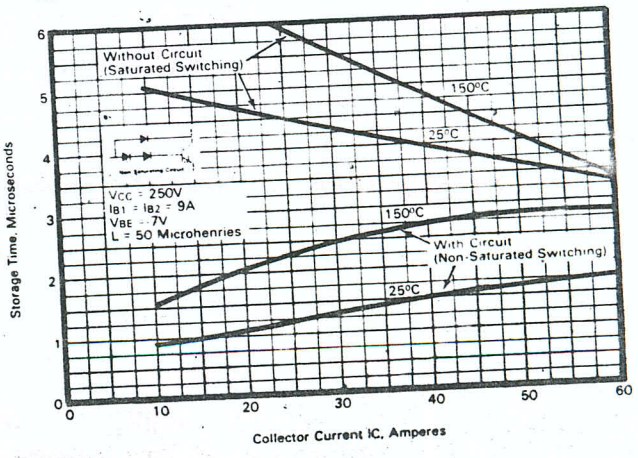
D62T_ _50 Typical Storage Time For Clamped Inductive Switching



D62T_ _60 Typical Turn-Off time For Clamped Inductive Switching



D62T_ _60 Typical Storage Time For Clamped Inductive Switching



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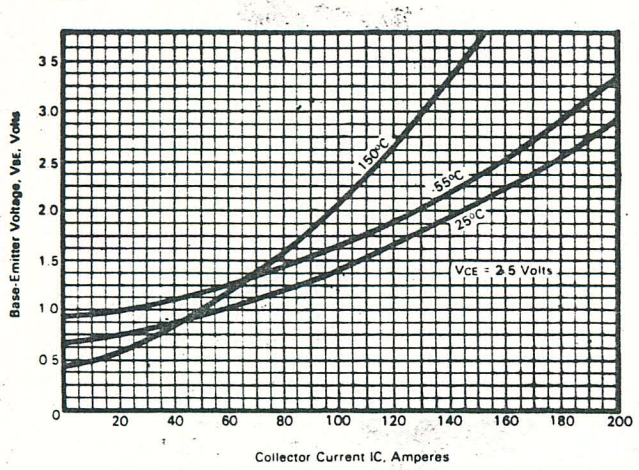
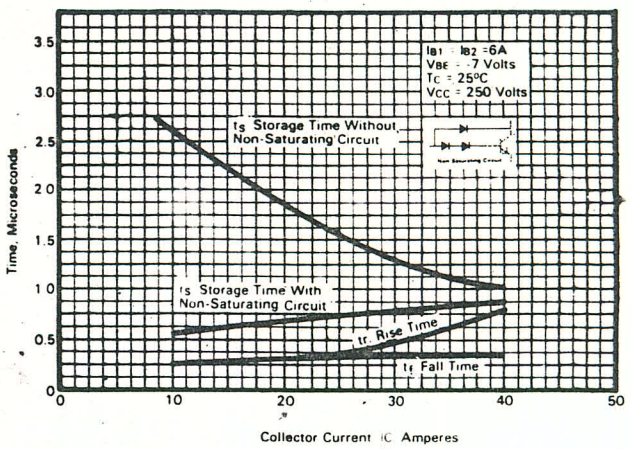
D62T_ _40

Typical Transfer Characteristics



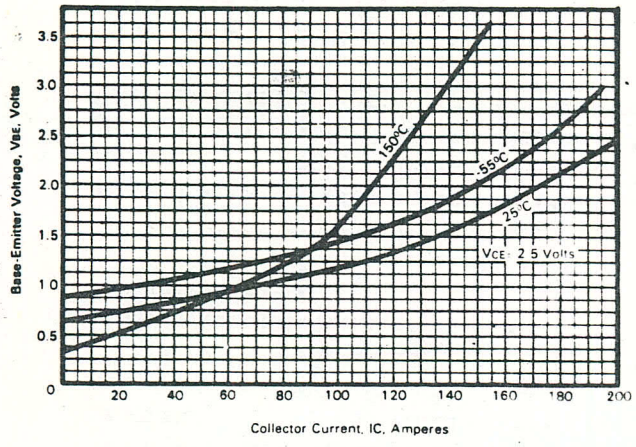
D62T_ _40

Typical Resistive Switching Times



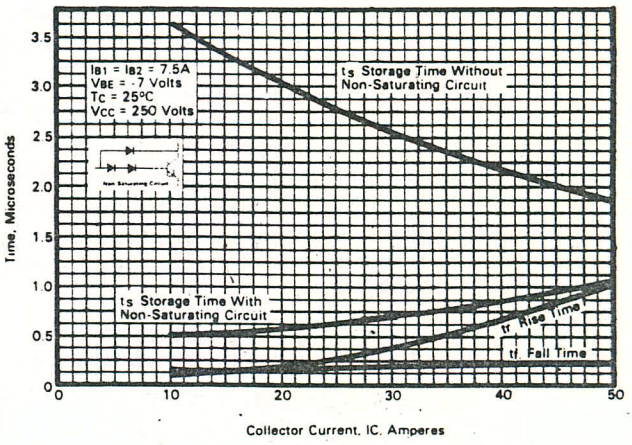
D62T_ _50

Typical Transfer Characteristics



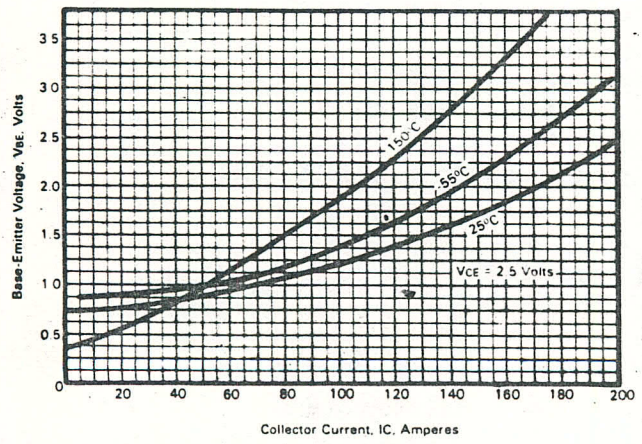
D62T_ _50

Typical Resistive Switching Times



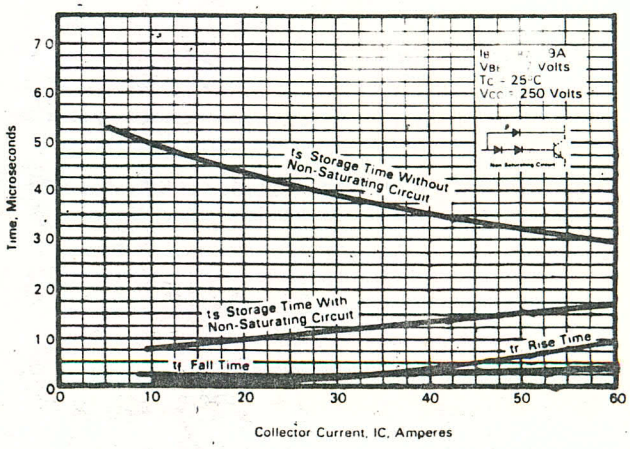
D62T_ _60

Typical Transfer Characteristics



D62T_ _60

Typical Resistive Switching Times



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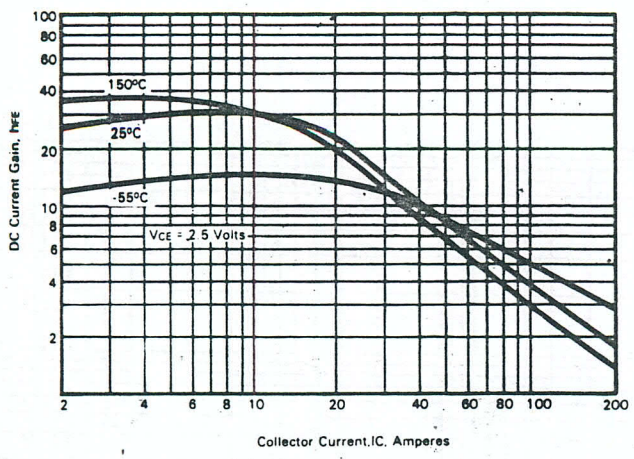
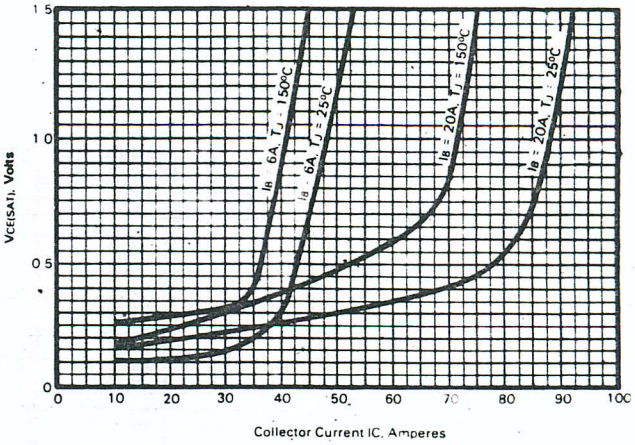
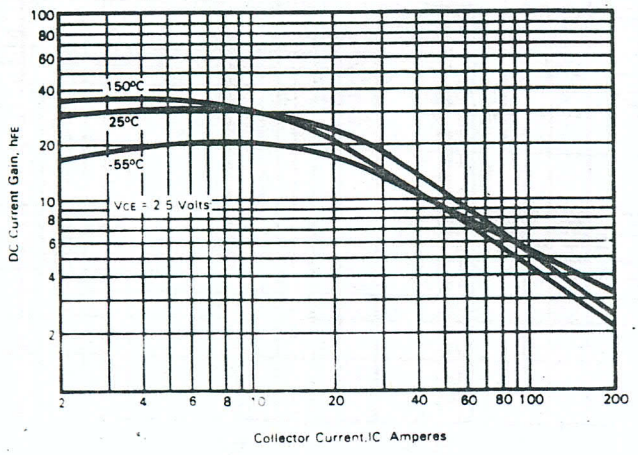
D62T_ _40 Typical DC Current Gain



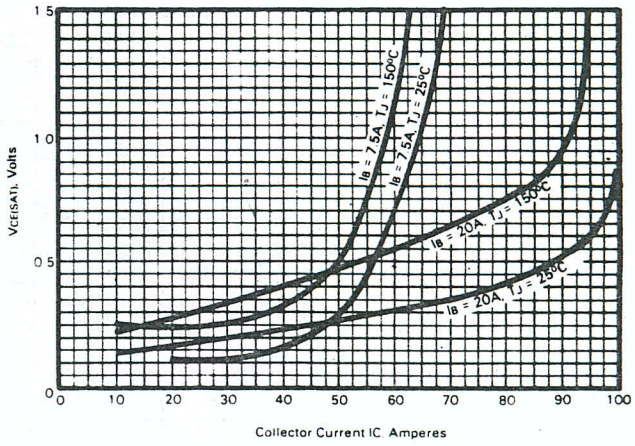
D62T_ _40 Typical Collector-emitter Saturation Voltage



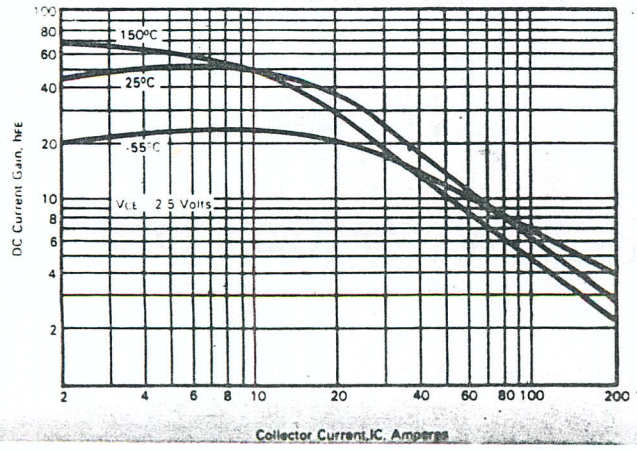
D62T_ _50 Typical DC Current Gain



D62T_ _50 Typical Collector-emitter Saturation Voltage



D62T_ _60 Typical DC Current Gain



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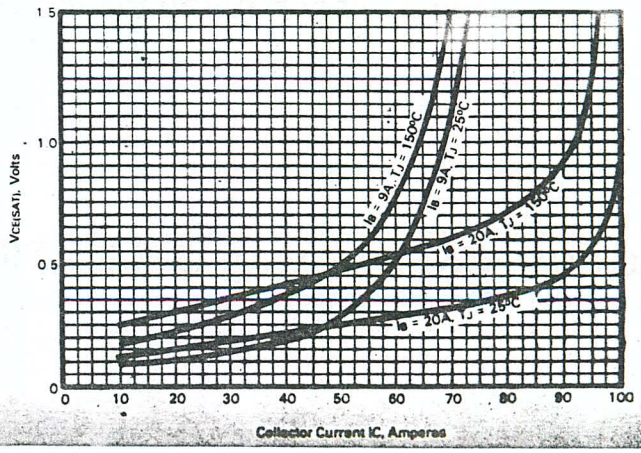

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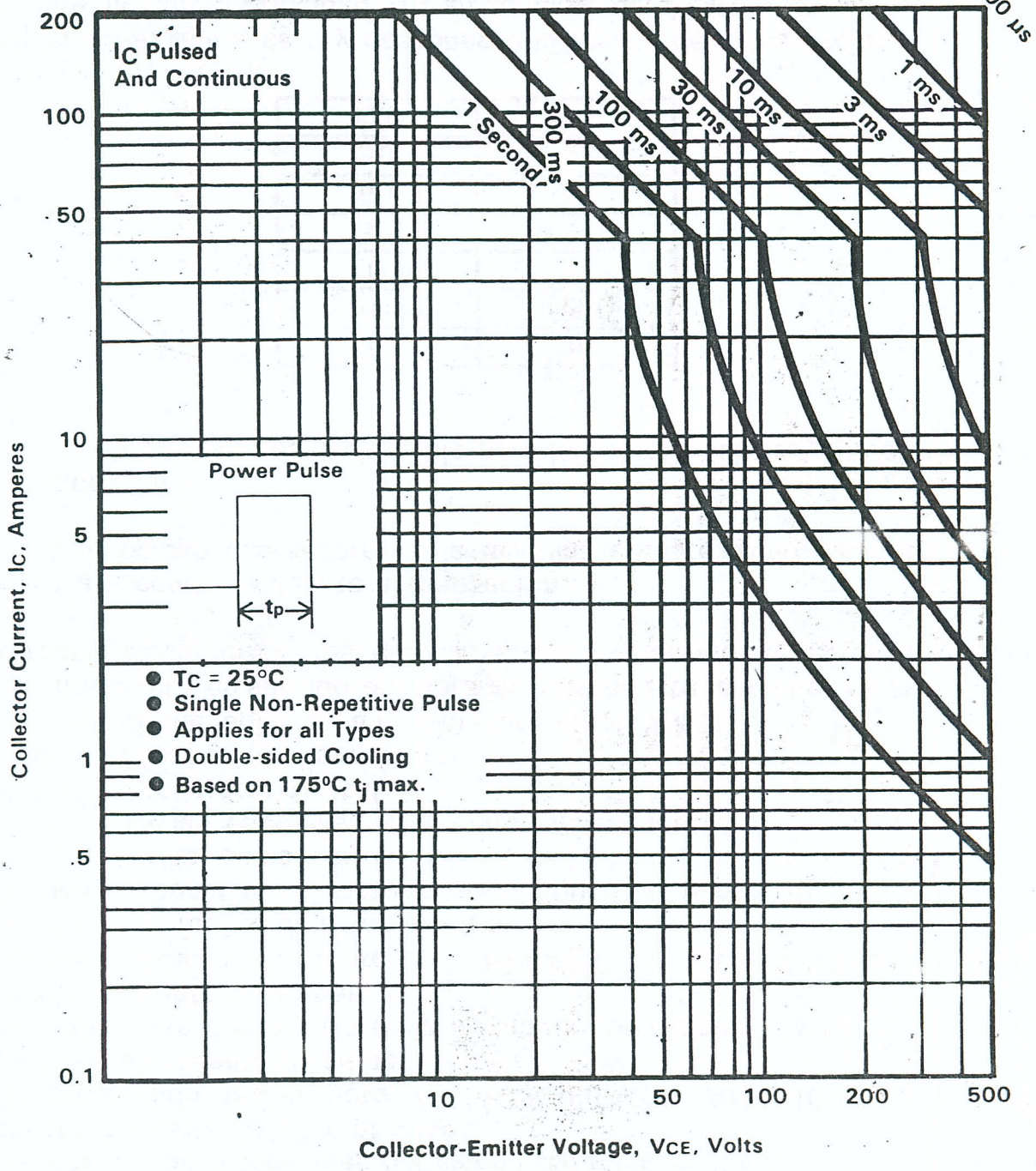
NPN Power Switching TRANSISTORS D62T

Maximum Forward Bias Safe Operating Area — S.O.A.



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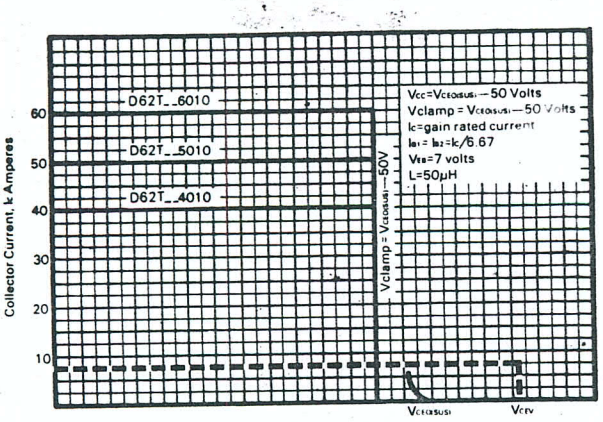
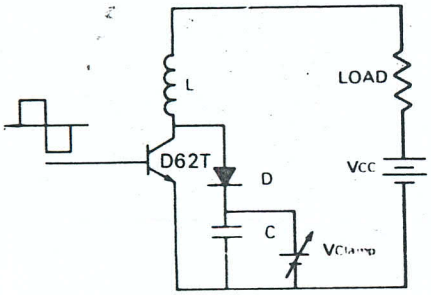
Reverse Bias Safe Switching Area



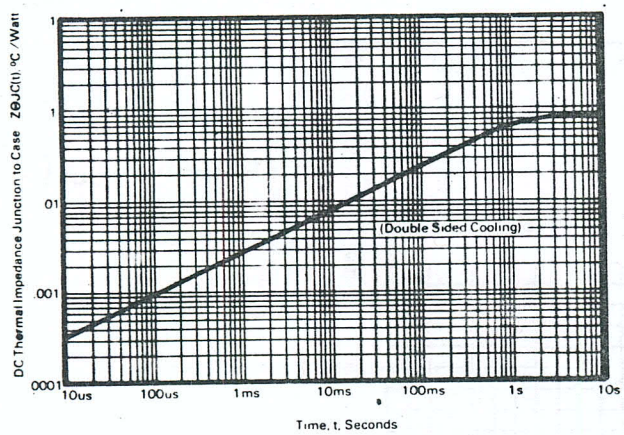


INDUCTIVE TURN-OFF CAPABILITY

All D62T transistors are tested in the clamped inductive circuit shown. This test is assurance that every D62T transistor is capable of switching clamped inductive loads traversing the load line as shown on the Reverse Bias Safe Switching graph.

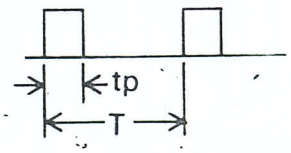
The dotted line on the Safe Switching Area is an additional test that can be done on all transistors. Consult the factory for this special test.

Transient Thermal Impedance Vs. Time



FORMULA TO DETERMINE SWITCH INTERVAL JUNCTION TEMPERATURE EXCURSIONS*

$$T_{max} = \left[\frac{tp\ Z\theta 1}{T} + \left[1 - \frac{tp}{T}\right] Z\theta 2 - Z\theta 3 + Z\theta 4\right] P + T_C$$



Zθ1 = ZθJC Steady State
Zθ2 = Transient Thermal Impedance of Time (T + tp)
Zθ3 = Transient Thermal Impedance of the Period T
Zθ4 = Transient Thermal Impedance of the Pulse Width tp
P = Peak Power During Switching
T_{max} = Maximum Junction Temperature
T_C = Case Temperature

* For further information consult factory.

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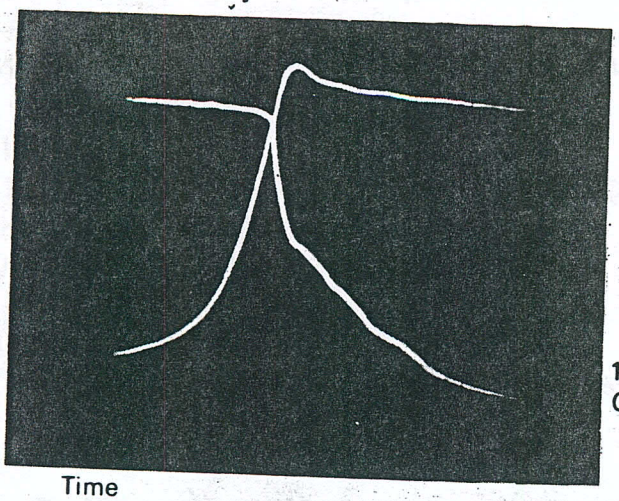
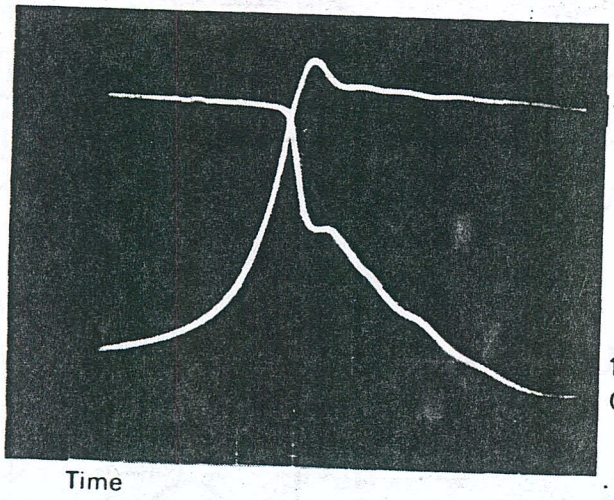
TYPICAL TURN-OFF WAVE FORMS FOR CLAMPED INDUCTIVE SWITCHING*

* Shown below are actual photographs taken during 150°C inductive switching measurements



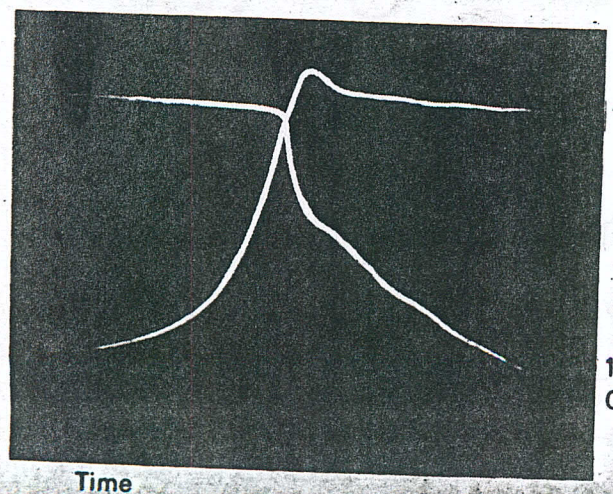
D62T_ _40

V_{CE} = 250V, 50V/cm
I_C = 50A, 10A/cm
$I_{B1} = I_{B2}$ = 6A, V_{EB} = 7V
time = 100ns/cm
T = 150°C



D62T_ _50

V_{CE} = 250V, 50V/cm
I_C = 50A, 10A/cm
$I_{B1} = I_{B2}$ = 7.5A, V_{EB} = 7V
time = 100 ns/cm
T = 150°C



D62T_ _60

V_{CE} = 250V, 50V/cm
I_C = 60A, scale not calibrated
$I_{B1} = I_{B2}$ = 9A, V_{EB} = 7V
time = 100ns/cm
T = 150°C